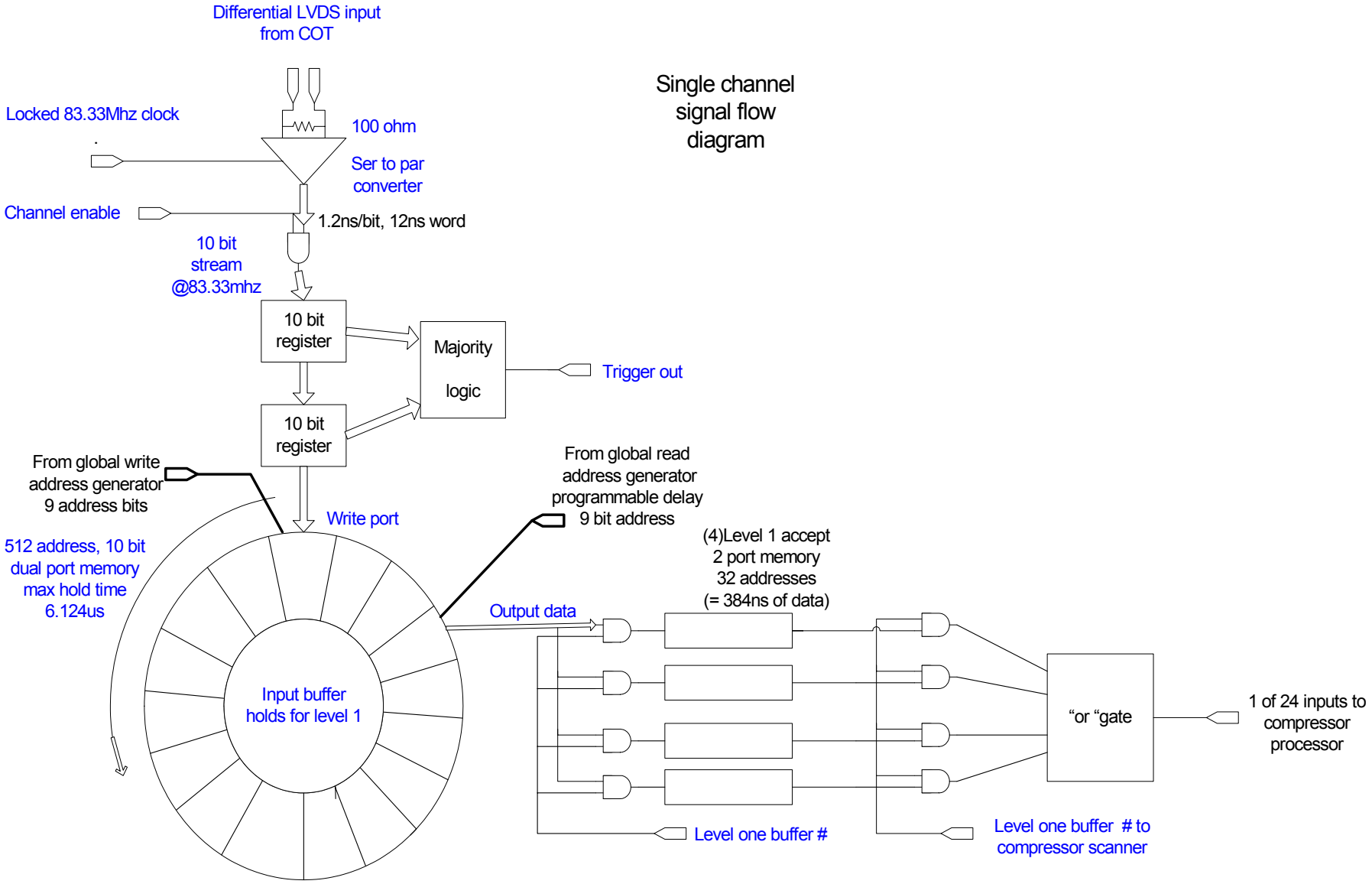
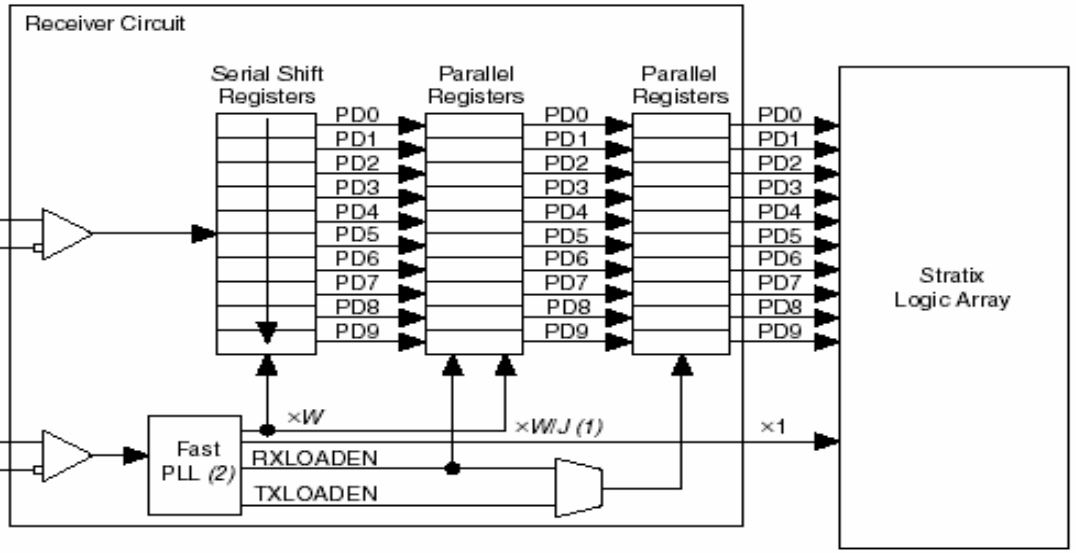

Single channel signal flow diagram
Differential LVDS input from COT
Locked 83.33Mhz clock
100 ohm
Ser to par converter
Channel enable
1.2ns/bit, 12ns word
10 bit stream @83.33mhz
10 bit register
Majority logic
Trigger out
10 bit register
From global write address generator 9 address bits
From global read address generator programmable delay 9 bit address
Write port
512 address, 10 bit dual port memory max hold time 6.124us
(4)Level 1 accept 2 port memory 32 addresses (= 384ns of data)
Output data
Input buffer holds for level 1
"or "gate
1 of 24 inputs to compressor processor
Level one buffer #
Level one buffer # to compressor scanner

# Details of LVDS Receiver

Input from COT

83.3Mhz clk

*Figure 3. Stratix High-Speed Interface Deserialized in ×10 Mode*

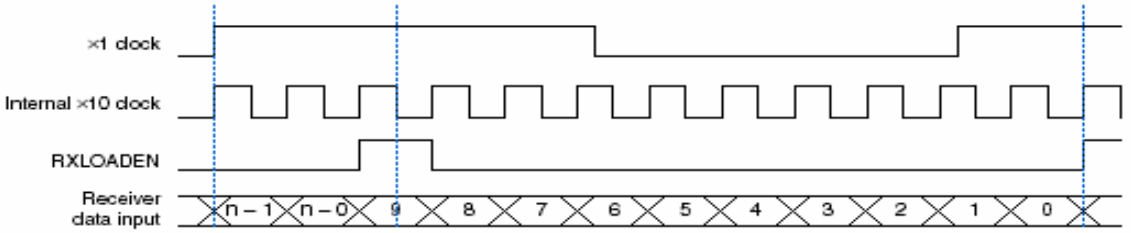



*Notes to Figure 3:*

(1) $W = 1, 2, 4, 8,$ or 10.
$J = 4, 8,$ or 10.
$W$ does not have to equal $J$. When $J = 1$ or 2, the deserializer is bypassed. When $J = 2$, the device uses DDRIO registers.

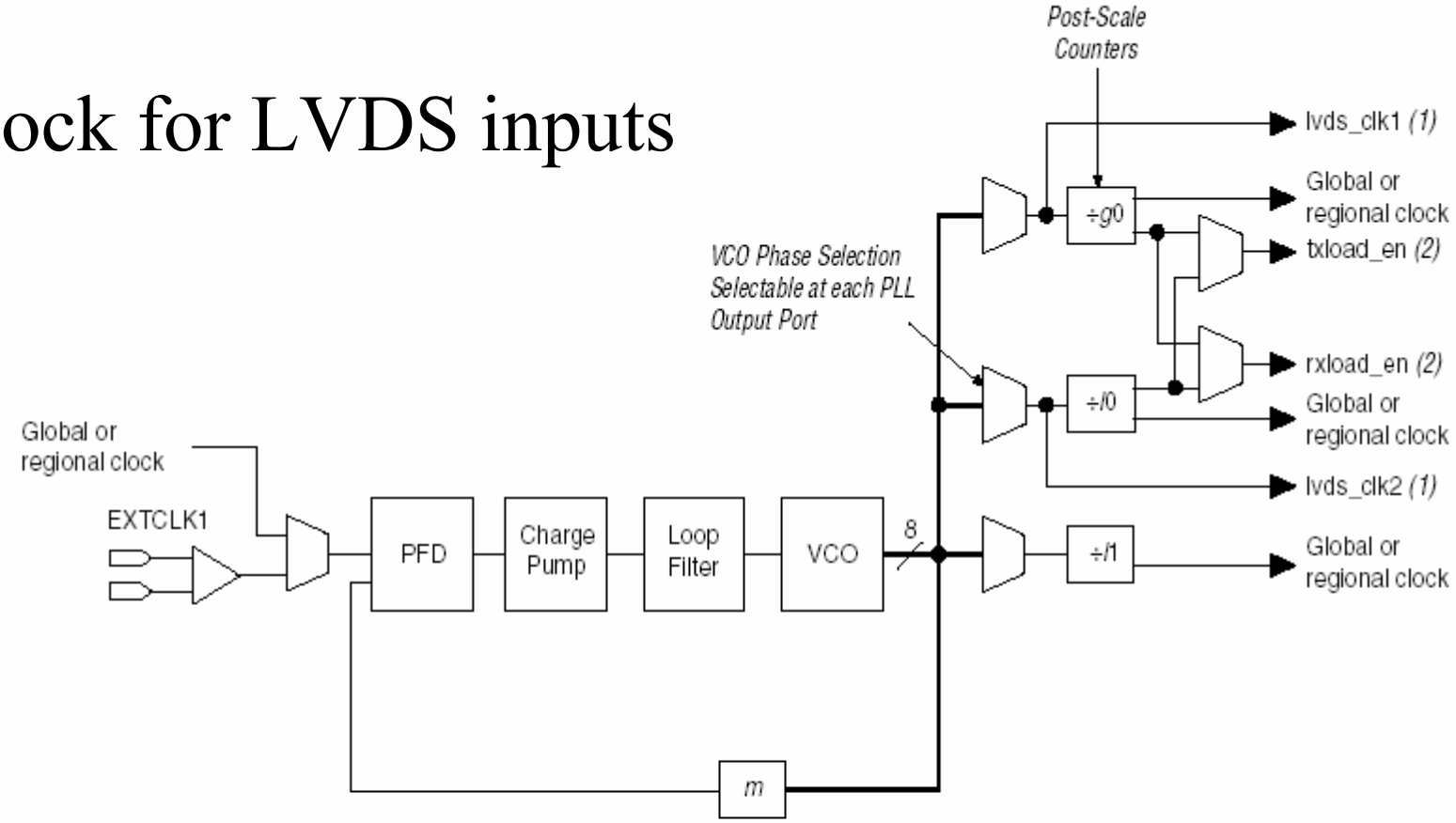
(2) This figure does not show additional circuitry for clock or data manipulation.

*Figure 4. Receiver Timing Diagram*



# Clock for LVDS inputs

*Figure 27. Stratix Fast PLL Block Diagram*

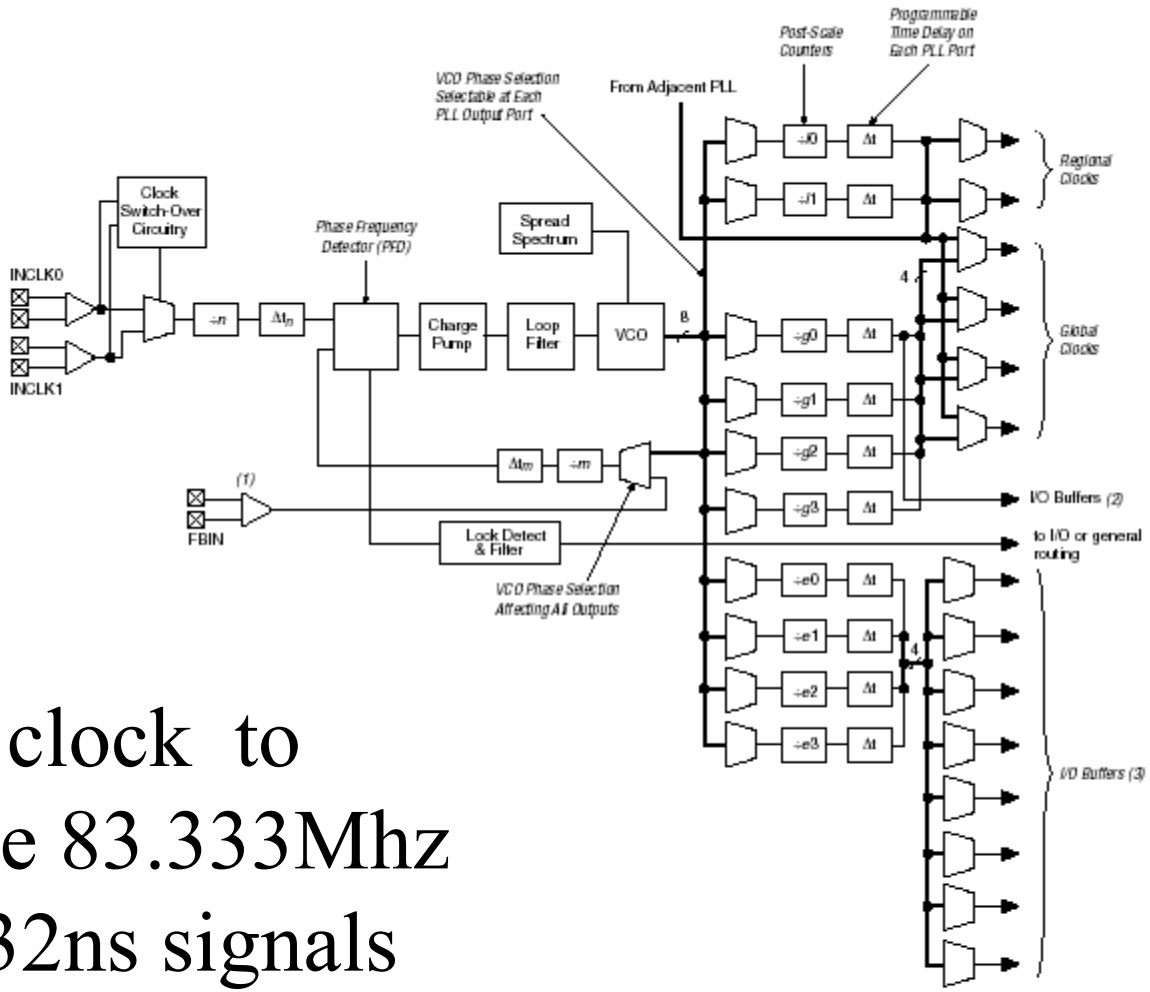



*Notes to Figure 27:*

(1) For high-speed differential I/O mode, the high-speed PLL clock feeds the serializer/deserializer (SERDES). Stratix devices only support one rate of data transfer per fast PLL in high-speed differential I/O mode.

(2) High-speed differential I/O SERDES control signal.

*Figure 2. Stratix Enhanced PLL*

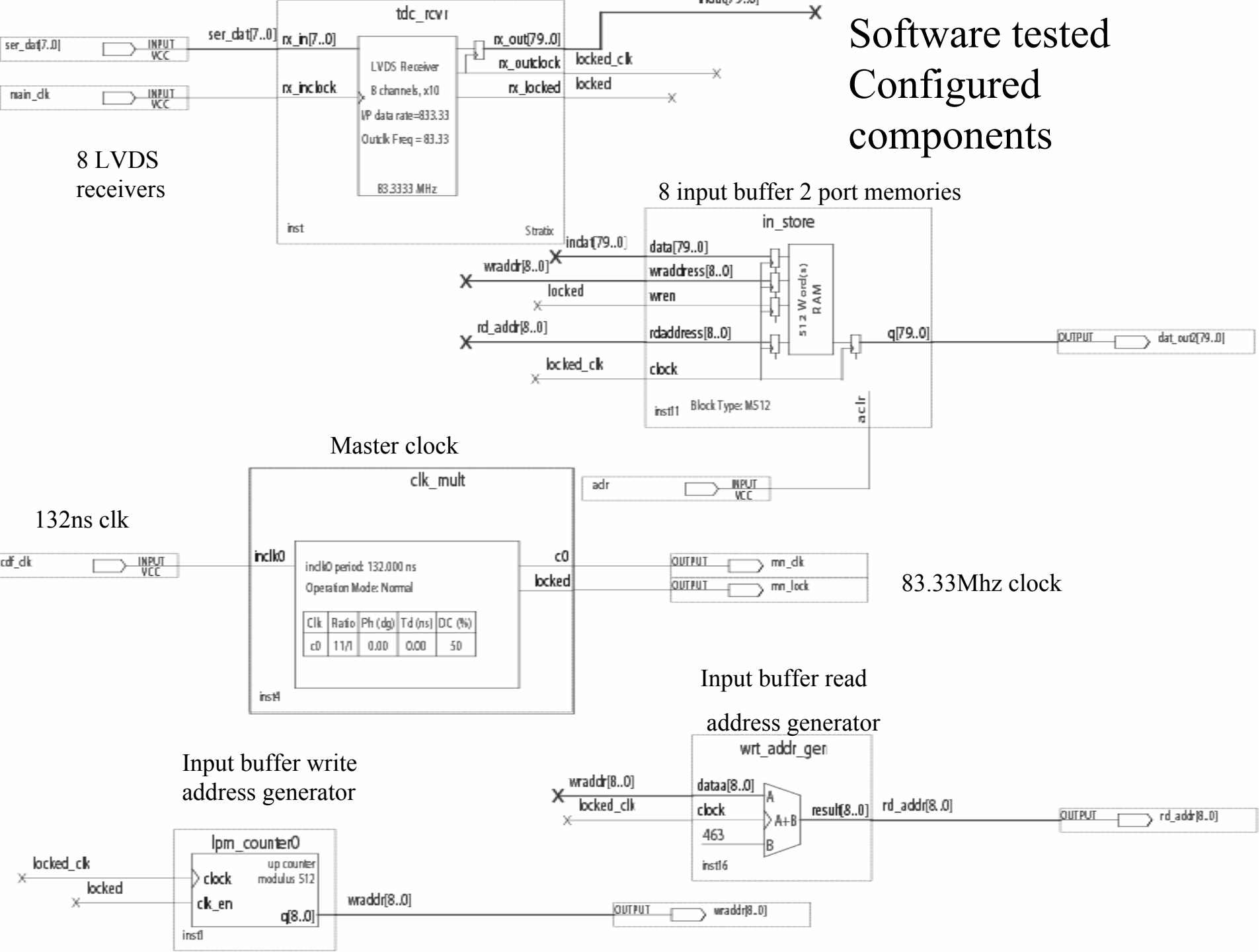


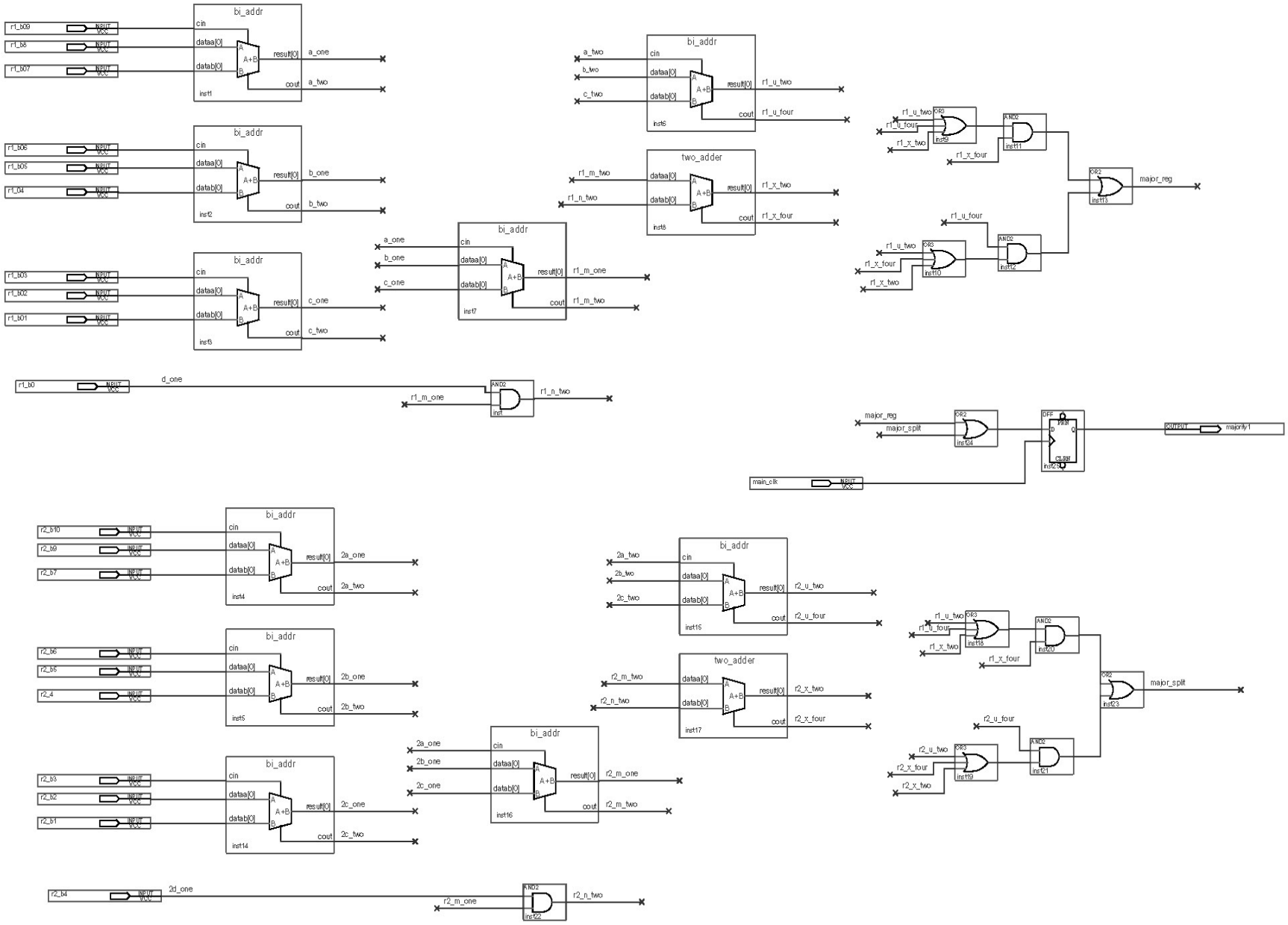

Master clock to generate 83.333Mhz from 132ns signals (X11)

*Notes to Figure 2:*

(1) External feedback is available in PLLs 5 and 6.
(2) This external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.

# Software tested Configured components




bi_addr
two_adder
r1_b09
r1_b08
r1_b07
r1_b06
r1_b05
r1_b04
r1_b03
r1_b02
r1_b01
r1_b0
a_one
a_two
b_one
b_two
c_one
c_two
d_one
r1_m_one
r1_n_two
r1_u_two
r1_u_four
r1_x_two
r1_x_four
major_reg
major_split
main_clk
majority1
r2_b10
r2_b09
r2_b07
r2_b06
r2_b05
r2_b04
r2_b03
r2_b02
r2_b01
r2_b0
2a_one
2a_two
2b_one
2b_two
2c_one
2c_two
2d_one
r2_m_one
r2_n_two
r2_u_two
r2_u_four
r2_x_two
r2_x_four

# SIMILAR SUCCESSFUL DESIGNS COMPLETED AT THE UNIVERSITY OF CHICAGO

All are 9U VME and have a VME interface (currently in use in CDF)
All include Altera FPGAS and required the same design tools

| BOARD | QUANTITY |
| --- | --- |
| Prefred | 10 |
| Dirac | 100 |
| Crate Sum | 16 |
| Track Fitter | 16 |
| Hit Finder | 50 |
| Flash ADC | 4 |
| Ghost Buster | 4 |